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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/672,551

09/26/2003

Seiji Funaba

17072

3724

23389 7590 07/19/2007  
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EXAMINER

SANDVIK, BENJAMIN P

ART UNIT

PAPER NUMBER

2826

MAIL DATE

DELIVERY MODE

07/19/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/672,551

Applicant(s)

FUNABA ET AL.

Examiner

Ben P. Sandvik

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 April 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-74 is/are pending in the application.
- 4a) Of the above claim(s) See Continuation Sheet is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13, 14, 17, 19, 23, 25, 31, 35 and 74 is/are allowed.
- 6) ☒ Claim(s) 1, 2, 5, 7, 55, 60, 61 and 72 is/are rejected.
- 7) ☒ Claim(s) 11 and 68 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

Continuation of Disposition of Claims: Claims withdrawn from consideration are 3,4,6,8-10,12,15,16,18,20-22,24,26-30,32-34,36-54,56-71 and 73.

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments filed 3/19/2007 have been fully considered but they are not persuasive. The examiner respectfully disagrees and submits that, as broadly interpreted, the Lin reference teaches all the limitations of the independent claims 1 and 55. Furthermore, there is no language in the claims that limits the claim to the "three way wiring connection" as argued by the applicant.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 55, and 72 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin (U.S. Patent #6383916).

With respect to **claim 1**, Lin teaches a semiconductor unit having two device terminals for every one input/output signal (Fig. 10, 101-105 and 121-125), said semiconductor unit comprising: a laminated substrate (Fig. 10, 130 and Col 7 Ln 21-23, the substrate is multi-layer) comprising at least two wiring layers which include a signal wiring layer and a power-supply or ground wiring

layer (Col 7 Ln 65-67), said laminated substrate having a main surface, a semiconductor chip (Fig. 10, 100) having an input/output pad (Fig. 5 and Col 6 Ln 21-23 and Fig. 7, 6) and being mounted on the main surface of said laminated substrate through said input/output pad, said two device terminals being mounted on said laminated substrate and being connected to both ends of a signal wire in said signal wiring layer (Fig. 10, 131), said signal wire being connected to the input/output pad of said semiconductor chip through a via hole (Fig. 7, 7').

With respect to **claim 55**, Lin teaches a semiconductor unit having at least two device terminals for every one input/output signal (Fig. 10, 101-105 and 121-125) said semiconductor unit having said two device terminals disposed in different sides of inside (Fig. 10, 122-124) and outside (Fig. 10, 121 and 125) of said semiconductor unit one by one, said two device terminals being wired (Fig. 10, 131) to an input/output pad of a semiconductor chip that corresponds to said input/output signal (Fig. 5 and Col 6 Ln 21-23 and Fig. 7, 6).

With respect to **claim 72**, Lin teaches a semiconductor unit comprising a semiconductor chip having an input/output pad (Fig. 10, 100) and a package having a main surface and a back surface (Fig. 10, 130), said package having at least two ball terminal adhesive areas for every one input/output signal on the main and back surfaces of said package (Fig. 10, area of wires 131 which are on the main and back surfaces of substrate 130 and connect to ball terminals), a ball terminal (Fig. 10, 101-105 and 121-125) being adhered to only one ball terminal adhesive area on one surface of said package; said two ball terminal adhesive

areas being connected to each through one of a via hole and a wire, said one of a via hole and a wire being connected to the input/output pad of said semiconductor chip through a wire (Fig. 10, the electrical connections 131 between the chip and the ball terminals comprise vias and wires).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, in view of Yew et al (U.S. Patent #6137164).

With respect to **claim 2**, Lin does not teach that the semiconductor chip comprises a circuit comprising at least one of an input buffer and an output buffer, an input protection resistor, and an electrostatic protection element. Yew teaches a chip having a layer of polymeric chip coating material (Col 6 Ln 39-41). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a layer of polymeric chip coating material to the chip of Lin as taught by Yew in order to give the chip electrostatic protection.

With respect to **claim 61**, Lin teaches a semiconductor unit having two device terminals for every one input/output signal (Fig. 10, 101-105 and 121-125), said semiconductor unit comprising: a laminated substrate (Fig. 10, 130

and Col 7 Ln 21-23, the substrate is multi-layer) comprising at least two wiring layers which include a signal wiring layer and a power-supply or ground wiring layer (Col 7 Ln 65-67), said laminated substrate having a main surface and a back surface, a semiconductor chip (Fig. 10, 100) having an input/output pad (Fig. 5 and Col 6 Ln 21-23 and Fig. 7, 6) and being mounted on the main surface of said laminated substrate, said two device terminals being disposed on the main surface (Fig. 10, 101-105) and the back surface (Fig. 10, 121-125) of said laminated substrate opposite to each other, and said signal wire being connected to the input/output pad of said semiconductor chip through a wire (Fig. 7, 7'); but Lin does not teach that there are two semiconductor chips mounted on main and back surfaces of said laminated substrate, or that said two device terminals are connected to each through a via hole. Yew teaches a substrate having two semiconductor chips mounted on the main surface and back surface respectively, the device terminals being connected to each other through a via hole (Fig. 5 and Abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide two semiconductor chips on the package of Lin as taught by Yew in order to improve the package density of the device (Col 3 Ln 25-29).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yew, in view of Devnani (U.S. Patent #6630628).

With respect to **claim 5**, Yew does not teach that the signal wiring layer forms a micro-strip line with the ground wiring layer in said laminated substrate, said ground wiring layer being disposed between said signal wiring layer and said semiconductor chip. Devnani teaches that the signal layer forms a micro strip line and that the ground wiring layer (Fig. 2, 140) is disposed between the signal layer (Fig. 2, 150) and the semiconductor chip (Fig. 2, 105). It would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the signal and ground layers of Yew as taught Devnani in order to optimize the wiring arrangement of the substrate.

Claims 7 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, in view of Tanahashi (U.S. Patent #6184477).

With respect to **claim 7**, Lin does not teach said signal wiring layer being sandwiched between the power-supply layer and the ground layer in said laminated substrate, said signal wiring layer forming a strip line with the power-supply layer or the ground layer. Tanahashi teaches a signal layer (Fig. 6, S1) between a power layer (Fig. 6, P) and a ground layer (Fig. 6, G), the signal layer forming a strip line (Fig. 5, S1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to arranged the wiring layers of Lin as taught by Tanahashi in order to optimize the electrical characteristics of the device.



With respect to **claim 60**, Lin teaches a semiconductor unit having two device terminals for every one input/output signal (Fig. 10, 101-105 and 121-125), said semiconductor unit comprising: a laminated substrate (Fig. 10, 130 and Col 7 Ln 21-23, the substrate is multi-layer) comprising at least two wiring layers which include a signal wiring layer and a power-supply or ground wiring layer (Col 7 Ln 65-67), said laminated substrate having a main surface, a semiconductor chip (Fig. 10, 100) having an input/output pad (Fig. 5 and Col 6 Ln 21-23 and Fig. 7, 6) and being mounted on the main surface of said laminated substrate through said input/output pad, said two device terminals being disposed on the main surface (Fig. 10, 101-105) and the back surface (Fig. 10, 121-125) of said laminated substrate opposite to each other, respectively, said signal wire being connected to the input/output pad of said semiconductor chip through a wire (Fig. 7, 7'); but Lin does not teach that said two device terminals are connected to each other through a via hole. Tanahashi teaches a substrate that has connections utilizing via holes (Fig. 6, T, TG, etc.). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use via holes in the substrate of Lin, hence the device terminals would be connected to each other through a via hole, in order to have proper insulation within the substrate (Col 10 Ln 5-8).

***Allowable Subject Matter***

Claims 13, 14, 17, 19, 23, 25, 31, 35, and 74 are allowed.

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Claims 11 and 68 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

bps

  
**EVAN PERT  
PRIMARY EXAMINER**